ILLIAC 6 (illiac6.cs.uiuc.edu)
Communications Supercomputer

PROCESSOR
Analog Devices Incorporated TigerSHARC 201
500MHz
4 x 1Gbyte/sec communication ports
4-wide VLIW
256 bits per cycle fixed point bandwidth
256 bits per cycle memory bandwidth
3Mbytes internal RAM

CARRIER BOARD
32 processors

CHASSIS
1024 processors

HARDWARE

SYSTEM NUMBERS

<table>
<thead>
<tr>
<th>processors</th>
<th>65536</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAM</td>
<td>2.3 terabytes</td>
</tr>
<tr>
<td>16-bit fixed point bandwidth</td>
<td>524 peta ops per second</td>
</tr>
<tr>
<td>32-bit floating point bandwidth</td>
<td>196 peta ops per second</td>
</tr>
<tr>
<td>max IO bandwidth</td>
<td>65 petabits per second</td>
</tr>
<tr>
<td>bisection bandwidth</td>
<td>65 petabits per second</td>
</tr>
<tr>
<td>IO media</td>
<td>SONET, gigabit Ethernet</td>
</tr>
<tr>
<td>power dissipation</td>
<td>less than 500kW</td>
</tr>
<tr>
<td>processor boards</td>
<td>2048</td>
</tr>
<tr>
<td>chassis</td>
<td>64</td>
</tr>
</tbody>
</table>

SUBSYSTEM
8192 processors

SYSTEM
65536 processors

Principal Investigator:
Luddy Harrison
luddy@uiuc.edu

Collaborators:
Analog Devices
Mentor Graphics
Xilinx

Additional industry collaborators welcome!
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MEZZANINE CARD
Four TigerSHARC 201 DSPs
One Xilinx Virtex (Virtex 2 Pro, later Virtex 4)
SDRAM

FUNCTIONS of the FPGA:
System interconnect fabric
Reconfigurable silicon
System I/O interfacing

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FIRMWARE FUNCTIONS
- Boot
- Diagnostic
- Debug
- Communication
  - Routing
  - Messaging
  - Shared Memory
  - Broadcast
  - Combining
- Synchronization
- Input / Output

APPLICATIONS
- Real-Time, One Look Stream Processing
- Stream Mining
- Software Radio
- Network Security
- Sensor Filtering
- Massive Multiplayer Games
- Real-Time Simulation
- Guaranteed Bandwidth Model (HW & SW)

SOFTWARE
- COMPONENT LIB
- APPLICATION

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Component A
Component B
Component C

200Mb/s
10Gb/s
10Gb/s
10Gb/s
20Gb/s
10Gb/s
20Gb/s

APPLICATION REALIZED MAPPED